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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/985,768 | 11/06/2001 | Kwame Osei Boateng | 826.1767 | 4333 |

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| EXAMINER | |
|---|---|
| SIEK, VUTHE | |
| **ART UNIT** | **PAPER NUMBER** |
| 2825 | |

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/985,768 | BOATENG, KWAME OSEI | |
| | Examiner | Art Unit | |
| | Vuthe Siek | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 09/985,768 and RCE with submission of amendment filed on 4/11/2006. Claims 1-14 remain pending in the application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5, 7, 9 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (5,771,243).

4. As to claims 1 and 10-13, Lee et al. teach a method of identifying redundant test patterns and then eliminating the redundant test patterns thereof (see summary, Figs. 1-2). The method comprising performing a simulation on a digital circuit with a set of test stimuli to trace faults which the set of test stimuli cover (testing an integrated circuit with set of test stimuli, col. 2 lines 25-46, Fig. 1, items 20-22); selecting essential test stimuli (test patterns from each sets or subsets) from among subsets of the set of test stimuli after mapping between the test stimuli and the faults has been established by the simulation, an essential test stimuli being a test stimulus that detects at least one fault,

which is detectable by no other test stimulus in one of the subsets of test stimuli (Col. 2 lines 25-46; Fig. 1, select results for test patterns); eliminating redundant test stimuli from among subsets of the test stimuli after selection of the essential test stimuli from each subset, a redundant test stimulus being a test stimulus that detects a fault, which is detectable by another test stimulus in each subset after the selection of the essential test stimuli; and outputting a compacted set (reduced set of test patterns) (col. 2 lines 47-65; Fig. 1, items 24-34). The process for testing an IC, selection of test patterns, eliminating of test patterns to create a reduced set of test patterns is performed by a software program operable on a computer.

5. As to claim 14, Lee et al. describes in Fig. 1, the claim limitations of selecting essential test stimuli (test patterns); and eliminating redundant test stimuli after selection of the essential test stimuli.

6. As to claim 2, Lee et al. teach outputting a reduced set of test patterns (a minimum-sized subset of the set of test stimuli), which covers faults detectable by the set of test stimuli without modifying test stimuli in the minimum-sized subset, as the compacted set (reduced set test patterns) (Fig. 1, Item 34).

7. As to claim 3, Lee et al. teach hierarchically repeating the selection of essential test stimuli (test patterns) from among subsets of remaining test stimuli after elimination of redundant rest stimuli from the subsets, and outputting the compacted set comprising the selected essential test stimuli (Fig. 2 in conjunction with Fig. 1, where Fig. 2 describes the repeated process of Fig. 1).

8. As to claim 4, Lee et al. teach the elimination includes identifying a subset of test stimuli (set or subset) that optimally covers a given set of faults and eliminating one or more test stimuli other than the identified test stimuli as the redundant test stimuli (Fig. 1; col. 2 lines 47-58).

9. As to claim 5, Lee et al. teach storing information of the set of test stimuli, information of faults which the set of test stimuli cover in matrix form as shown in Figs. 4-6. Pointing information associating each test stimuli with the faults detectable by a corresponding test stimuli must be also be stored, so that such information must be used by process of selecting and eliminating as described in Figs. 1-2.

10. As to claim 7, Lee et al. teach stuck fault test pattern generation (col. 1 lines 22-53).

11. As to claim 9, Lee et al. teach performing compaction of the set of test stimuli by regarding a sequence of initializing, sensitizing and propagation subsequences as a single test stimulus (Fig. 1).

12. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Unnikrishnan et al. (6,810,372 B1).

13. As to claim 14, Unnikrishnan et al. teach substantially the same claim invention comprising selecting step and eliminating redundant test stimuli after selection of the essential test stimuli (Fig. 3, selecting step 204 is before deleting step 211).

14. Claims 1-5 and 7-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kajihara et al., "Cost-Effective Generation of Minimal Test Sets for Stuck-at Faults in Combinational Logic Circuits," IEEE, Dec. 1995, pp. 1496-1504.

15. As to claims 1 and 10-13, Kajihara et al. teach new cost-effective heuristics for a generation of minimal test sets (compacted set of test stimuli) for a digital circuit (see whole article) comprising fault simulation under double detection (starting page 1498, section D.); selecting essential test stimuli from among subsets of the set of test stimuli after mapping between the test stimuli and the faults has been established by the simulation, where an essential test stimulus being a test stimulus that detects at least one fault, which is detectable by no other test stimulus in one of the subsets of the test stimuli (page 1500, section III. A STATIC COMPACTION TECHNIQUE, especially section A. describes mapping between test stimuli and faults for example consider five faults: {f1, f2, f3, f4, f5}; suppose that three test vectors t1,t2 and t3 are generated; let det(t1) = {f1,2,f3}; det(t2) = {f3, f4}; and det(t3) = {f5}); an eliminating redundant test stimuli form among subsets of test stimuli after selecting the essential test stimuli from each subset (page 1500, section III. A STATIC COMPACTION TECHNIQUE, especially section B., describing how to remove or eliminating redundant test stimuli in order to form a smaller subset of test stimuli; section A describes test vectors t2 and t3 are removed from the test set making test set become smaller); and an output device outputting a compacted set comprising the selected essential test stimuli (see at least section III. A STATIC COMPACTION TECHNIQUE starting page 1500, especially Table IV shows an output result). The redundant test stimulus is a test stimulus that detects a fault, which is detectable by another test stimulus in each subset after the selection of the essential test stimuli (section 2. page 1499, see Table IV).

16. As to claims 2-5 and 7-9, Kajihara et al., teach outputting a minimum-sized subset of the set of test stimuli, which covers faults without modifying test stimuli in the minimum-sized subset, as the compacted set; hierarchically repeating selecting of essential test stimuli after eliminating of redundant test stimuli to output the compacted set comprising the selected essential test stimuli; identifying a subset of test stimuli that optimally covers a given set of faults and eliminating one or more test stimuli other than the identified test stimuli as the redundant test stimuli; storing information of faults which the set of test stimuli cover, and pointing information associating each test stimulus with the faults detectable by a corresponding test stimulus; the faults including a stuck-at fault and a delay fault; performing compaction of the set of test stimuli by regarding a sequence of initializing, sensitizing, and propagation subsequences as a single test stimulus (See at least Section III, Table IV).

17. As to claim 14, Kajihara et al. teach a method for tracing faults on a circuit comprising selecting essential test stimuli; and eliminating test stimuli after selection of said essential test stimuli. Specifically, Kajihara et al. at least teach the selection pair of test vectors to be removed must be done as effectively and as accurately as possible, to ensure the cost-effectiveless of the procedure. This is especially important in view of the large number of pairs of test vectors that can be used as candidates for removal (page 1501, section B). The teachings meet the claim limitations. The selection of test vectors and then the removal of test vectors there after.

***Claim Rejections - 35 USC § 103***

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claim 6 is rejected under 35 U.S.C. 103(a) as being obvious over Kajihara et al., "Cost-Effective Generation of Minimal Test Sets for Stuck-at Faults in Combinational Logic Circuits," IEEE, Dec. 1995, pp. 1496-1504.

20. As to claim 6, Kajihara et al. teach using a fault simulation to search and detect essential faults of a test in the test set. As shown in Table IV, number of test of the test set, number of faults and number of check are described. It is well known to practitioners in the art that a counter is used to store information related application in order to facilitate a process of increasing or decreasing an information number stored in the counter. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to have stored counter information as recited in the claim in order to facilitate the fault simulation to obtain information as shown in Table IV as expected, thereby a compacted set comprising of essential test stimuli is finally obtained.

***Remarks***

21. Examiner has maintained the rejection under Kajihara. Applicant argued that Kajihara mainly does not teach selection of essential test vectors and then removal of redundant test vectors after selection. Examiner disagrees. Kajihara teaches the claim

limitations. One can understand that the removal cannot be done before selection. Nothing to remove if there is no selection. It is logically true that the selection must be done before done removal. Kajihara teaches double detection and triple detection to improve computation time. For example, Kajihara teaches in section A., page 1500, where the test vectors t2 and t3 can be removed because these test vectors are redundant test vectors. The test set is now become smaller {t1, t4} than {t1, t2, t3}. Kajihara does not teach away from the invention because Kajihara clearly teaches selecting essential test vectors and eliminating the redundant test stimuli after selection of the essential test stimuli. In addition, page 1501, Kajihara clearly teaches selection of essential test vectors and then eliminating redundant test vectors.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER